Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A process for management of a Test Access Port (TAP) function in a plurality of components arranged on a single chip, each of said components provided with a respective TAP function adapted to be driven by a respective dedicated clock and by at least one further signal, comprising the operations of:

using said at least one further signal in a shared way between the TAP functions of the plurality of components;

generating a clock signal for each component of the plurality of components using a dedicated clock generator for each clock signal; and

selectively driving the TAP functions of the plurality of components with a respective dedicated clock.

2. (Previously Presented) The process of claim 1, comprising the operations of:

associating, with said respective dedicated clock generator, a pull-down function.

3. (Previously Presented) The process of claim 2, comprising the operations of providing a common line for application of each clock signal to the TAP functions of the plurality of components.

4. (Previously Presented) The process of claim 2, comprising the operation of generating each clock signal on board said single chip.

5. (Previously Presented) A system for management of a Test Access Port (TAP) function in a plurality of components arranged on a single chip, each of the components provided with a respective TAP function adapted to be driven by a respective dedicated clock signal, comprising:

at least one line for use of at least one further signal in a shared way between the TAP functions of the plurality of components; and

a plurality of dedicated clock generators on the single chip, each clock generator generating a dedicated clock signal for selectively driving a respective TAP function in a respective component of the plurality of components.

6. (Previously Presented) The system of claim 5, comprising:

at least one pull-down module associated with said respective dedicated clock generators.

7. (Previously Presented) The system of claim 6, comprising a common line for the application of each clock signal to the TAP functions of the plurality of components.

8. (Previously Presented) The system of claim 6, wherein said dedicated clock generators are arranged on the single chip.

9. (Previously Presented) A method of managing a Test Access Port (TAP) function in conjunction with a plurality of components on a single chip, comprising:

providing each component of the plurality of components with a respective TAP function;

providing each TAP function of the plurality of components with a dedicated clock signal generated by a dedicated clock generator on the single chip;

providing at least one shared line for use by at least one further signal among the TAP functions of the plurality of components; and

selectively driving the respective TAP functions of the plurality of components with a respective dedicated clock signal.

10. (Previously Presented) The method of claim 9, wherein providing each TAP function with a respective dedicated clock signal comprises generating respective dedicated clock signals for the TAP functions of each component of the plurality of components.

11. (Previously Presented) The method of claim 10, wherein providing each TAP function with a respective dedicated clock signal comprises associating with each respective dedicated clock signal a pull-down function.

12. (Previously Presented) The method of claim 11, wherein providing each TAP function with a respective dedicated clock signal comprises providing a common line for use by each of the respective dedicated clock signals.

13. (Previously Presented) The method of claim 12, wherein each respective dedicated clock signal is generated onboard the single chip by a dedicated clock signal generator.

14. (Previously Presented) A system for managing testing of a plurality of components arranged on a single chip, the system comprising:

a Test Access Port (TAP) function associated with each component of the plurality of components on the single chip;

a plurality of clock generators on the single chip, each clock generator associated with a respective TAP function for selectively driving the TAP function with a respective dedicated clock signal; and

at least one shared line coupled to each component of the plurality of components and configured to carry at least one further signal.

15. (Original) The system of claim 14, further comprising at least one pull-down module associated with each respective clock generator and configured to generate a pull-down function.

16. (Original) The system of claim 15, further comprising a common line coupled to each of the respective clock generators and to each of the respective components of the plurality of components for selectively carrying each of the respective clock signals.

17. (Original) The system of claim 16, wherein each of the plurality of clock generators are provided on the signal chip.

18. (New) A process for management of a Test Access Port (TAP) function in a plurality of components arranged on a single chip, each of said components provided with a respective TAP function adapted to be driven by a respective dedicated clock and by at least one further signal, comprising the operations of:

using said at least one further signal in a shared way between the TAP functions of the plurality of components;

generating a clock signal for each component of the plurality of components using a dedicated clock generator for each clock signal; and

selectively driving the TAP functions of the plurality of components with a respective dedicated clock and associating, with said respective dedicated clock generator, a pull-down function.

19. (New) A system for management of a Test Access Port (TAP) function in a plurality of components arranged on a single chip, each of the components provided with a respective TAP function adapted to be driven by a respective dedicated clock signal, comprising:

at least one line for use of at least one further signal in a shared way between the TAP functions of the plurality of components;

a plurality of dedicated clock generators on the single chip, each clock generator generating a dedicated clock signal for selectively driving a respective TAP function in a respective component of the plurality of components; and

at least one pull-down module associated with said respective dedicated clock generators.

20. (New) A method of managing a Test Access Port (TAP) function in conjunction with a plurality of components on a single chip, comprising:

providing each component of the plurality of components with a respective TAP function;

providing each TAP function of the plurality of components with a dedicated clock signal generated by a dedicated clock generator on the single chip, and associating with each respective dedicated clock signal a pull-down function;

providing at least one shared line for use by at least one further signal among the TAP functions of the plurality of components; and

selectively driving the respective TAP functions of the plurality of components with a respective dedicated clock signal.

21. (New) A system for managing testing of a plurality of components arranged on a single chip, the system comprising:

a Test Access Port (TAP) function associated with each component of the plurality of components on the single chip;

a plurality of clock generators on the single chip, each clock generator associated with a respective TAP function for selectively driving the TAP function with a respective dedicated clock signal;

at least one shared line coupled to each component of the plurality of components and configured to carry at least one further signal; and

at least one pull-down module associated with each respective clock generator and configured to generate a pull-down function.